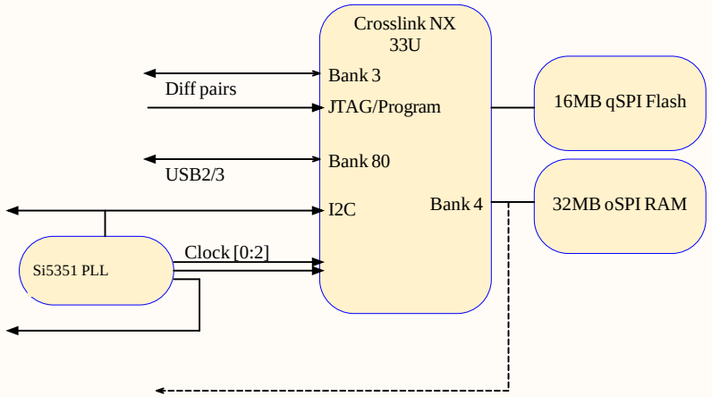
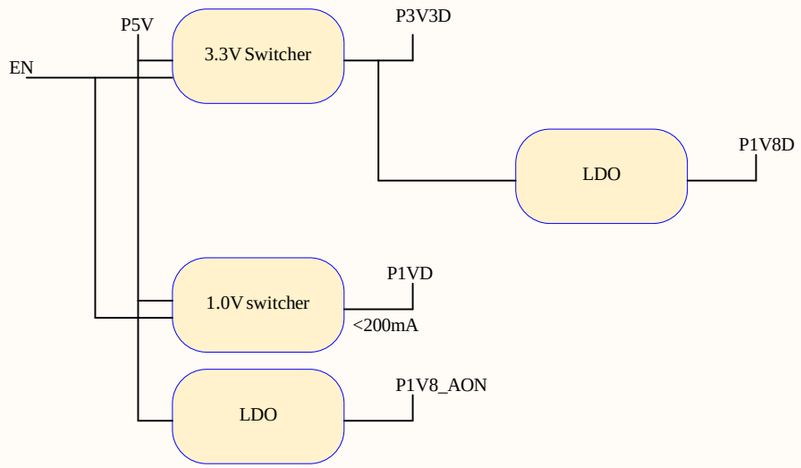
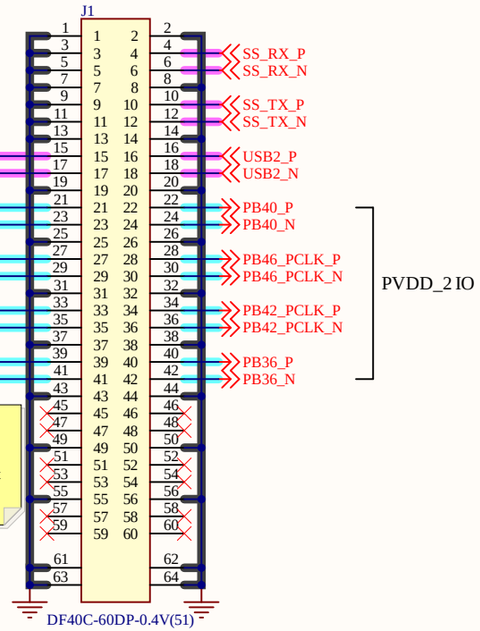
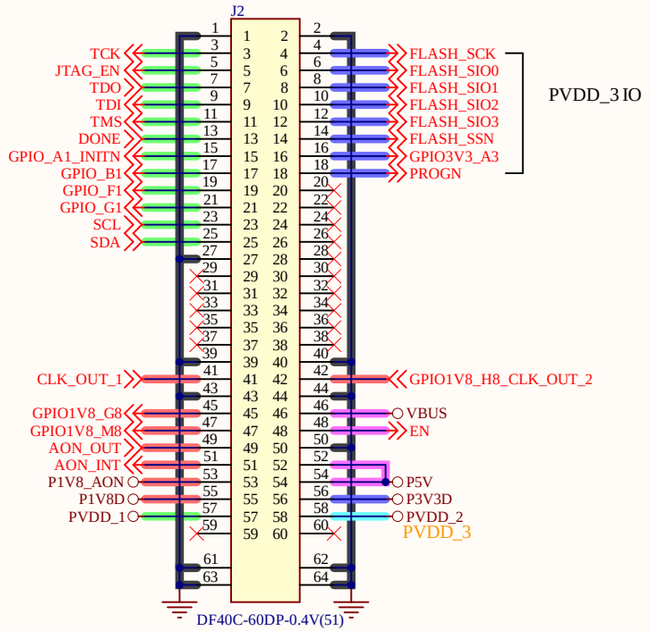

Crosslink NX
33U
Bank 3
Diff pairs
JTAG/Program
Bank 80
USB2/3
I2C
Bank 4
Clock [0:2]
Si5351 PLL
16MB qSPI Flash
32MB oSPI RAM


P5V
P3V3D
EN
3.3V Switcher
LDO
P1V8D
P1VD
1.0V switcher
<200mA
LDO
P1V8_AON

Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Ground



Reserved for Future use:
These signals will end up allocated to Bank 3 and the whole bank will be brought out to these pins when there is no SSRAM installed.

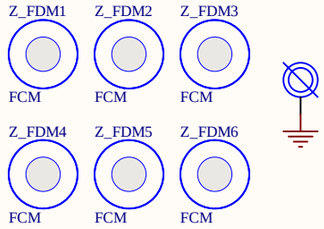


TODO:

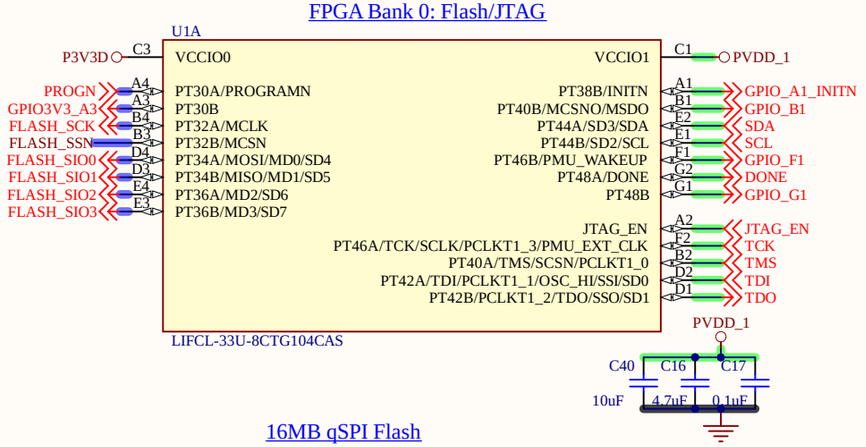
Note:
AON_INT will usually be connected to the EN pin on the board using a series resistor. This will enable PWM mode which isnt as efficient as the PWM mode.
To enable PWM mode, a high side switch needs to be implemented on the baseboard.

Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V

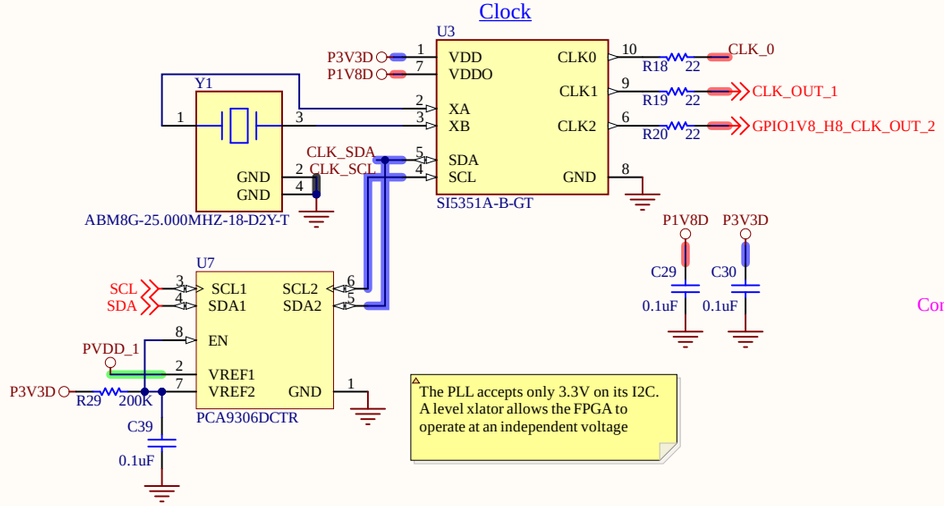
Layout note: Match diff pairs to within 1mm of each other.



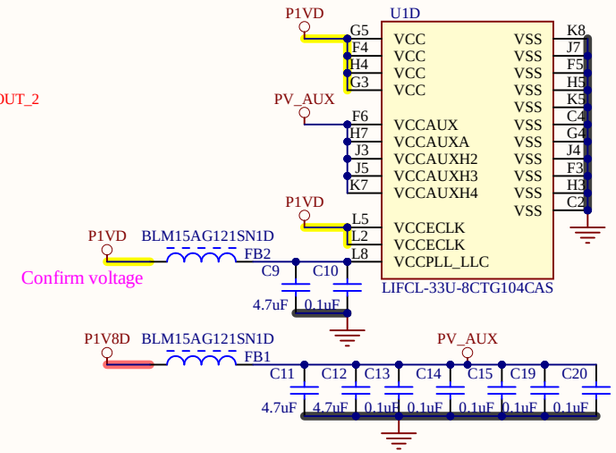
FPGA Bank 0: Flash/JTAG



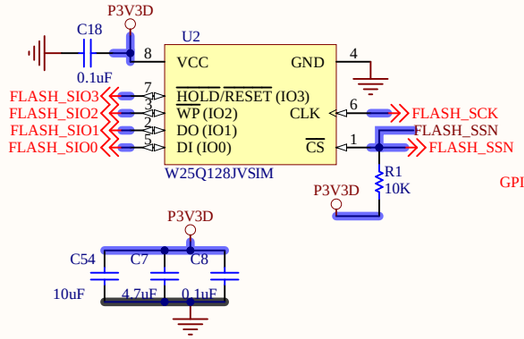
Clock



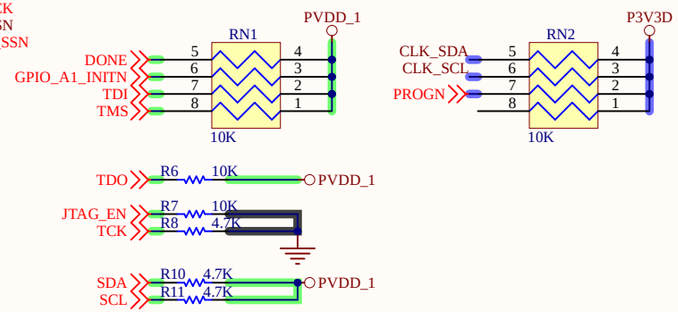
Power/Ground



16MB qSPI Flash

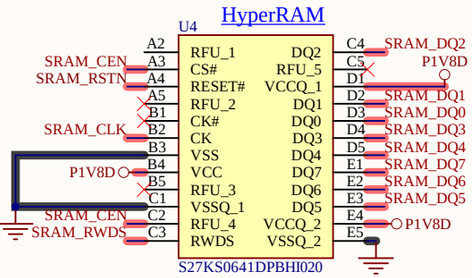


I2C and JTAG Pullups



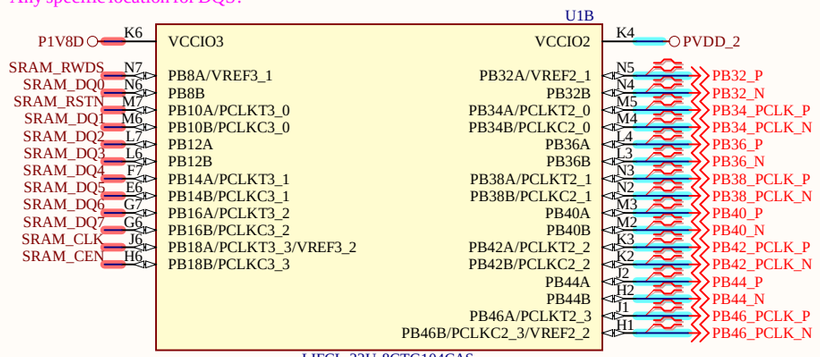
Bank 3: 32MB oSPI/HyperRAM

HyperRAM

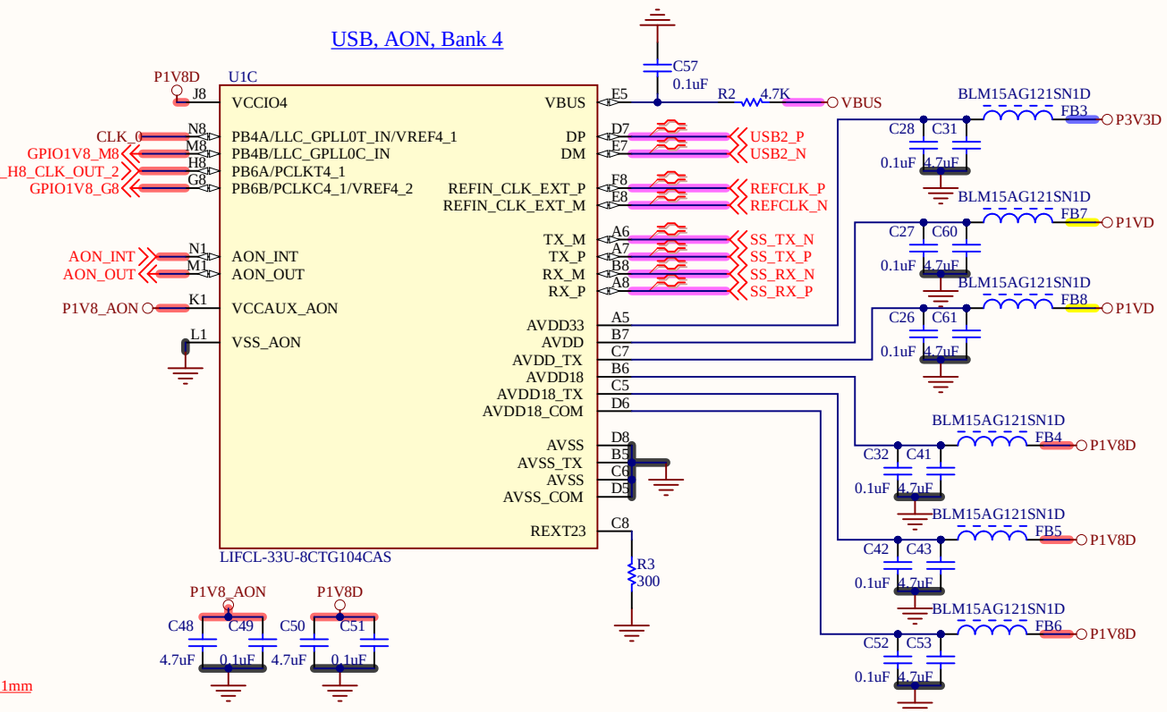


Any specific location for DQS?

Bank 2: External Interface



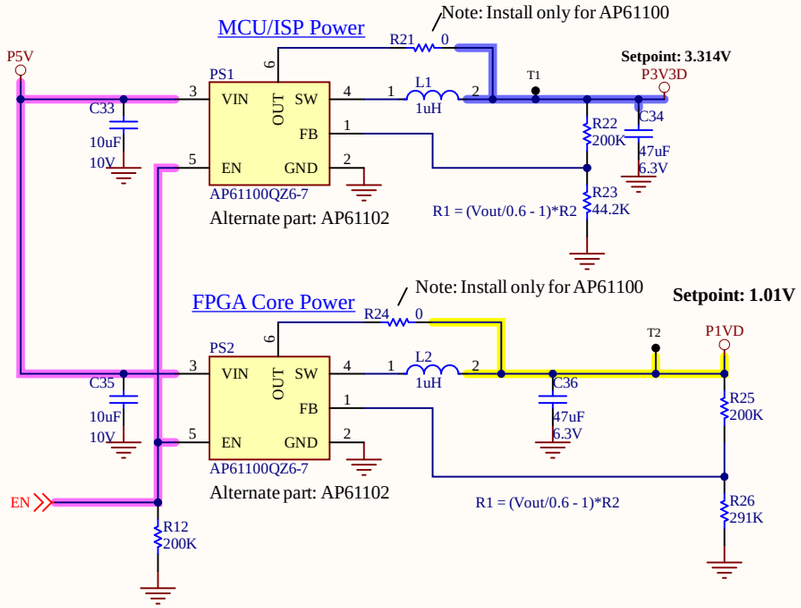
USB, AON, Bank 4



Layout: Length match SRAM_CLK to data lanes within 0.1mm

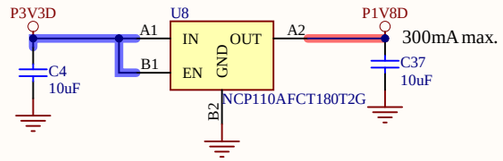
Layout: Length match all Bank 2 diff pairs with 1mm

MCU/ISP Power



FPGA Core Power

1.8V Power



1.8V Always On