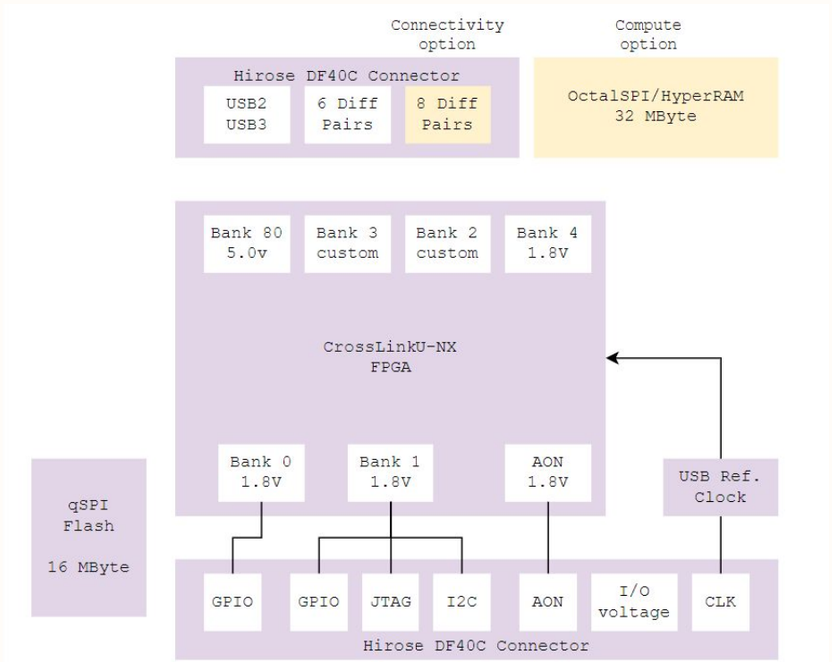
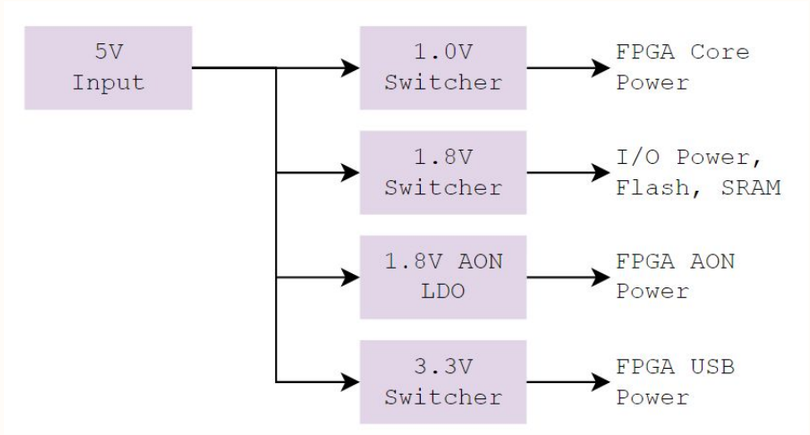
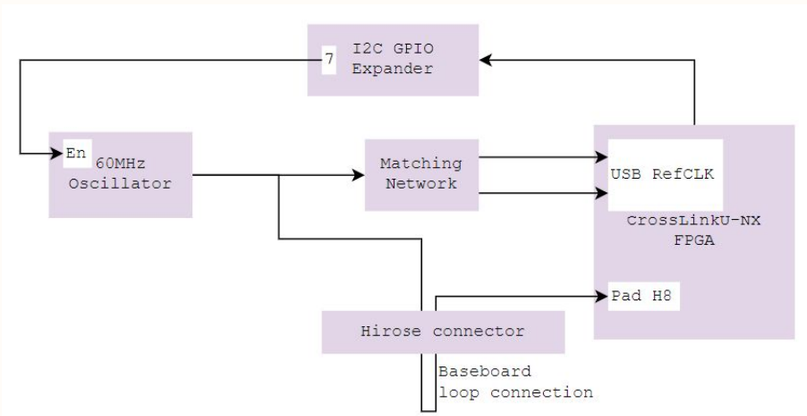
FPGA Bank Allocation



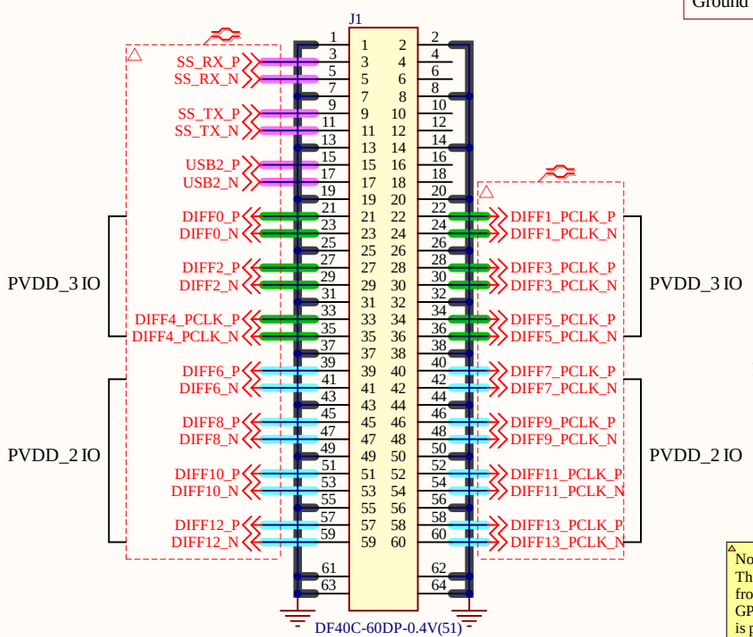
Power Distribution

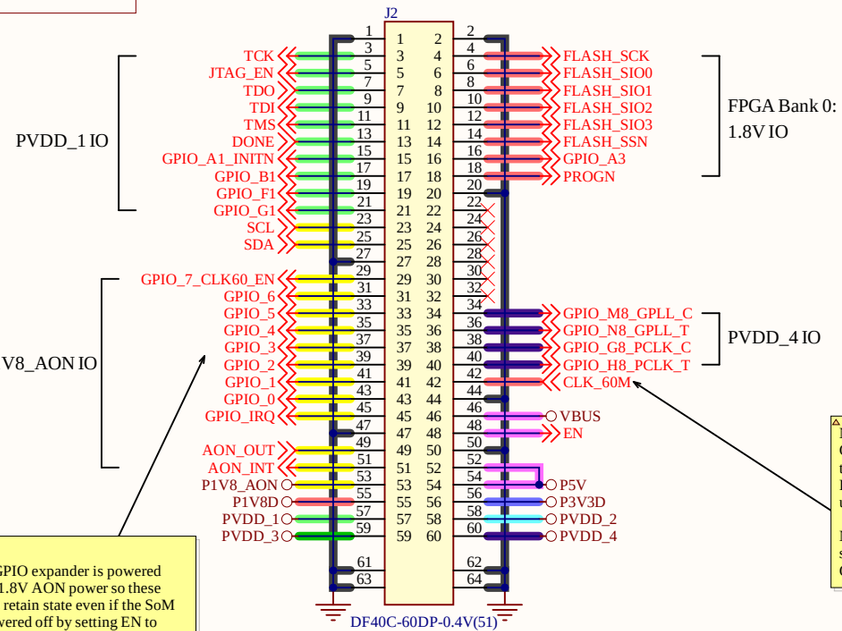


Clocking



Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Bank 3 Voltage (1.2-1.8V)
Always ON (1.8V)
Ground

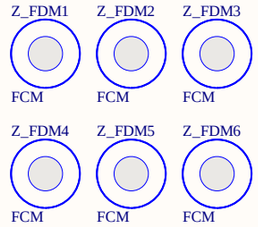




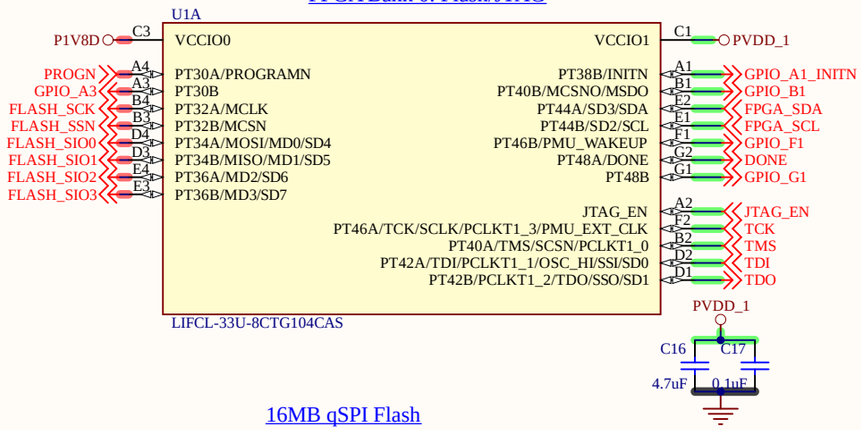
Note:
The GPIO expander is powered from 1.8V AON power so these GPIO retain state even if the SoM is powered off by setting EN to low.

Note:
Connect CLK_60 to GPIO_H8_PCLK_T on the baseboard to enable the onboard oscillator to send a clock to the FPGA. An external clock can be supplied to the FPGA using the H8 pin.

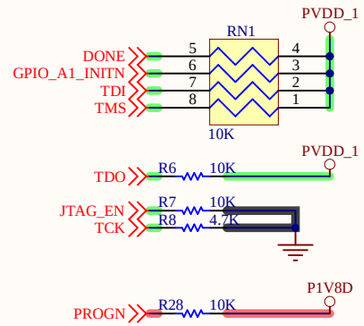
Note that since the CLK_60 uses 1.8V levels, PVDD_4 shall be set to 1.8V if the CLK_60 is connected to GPIO_H8_PCLK_T.



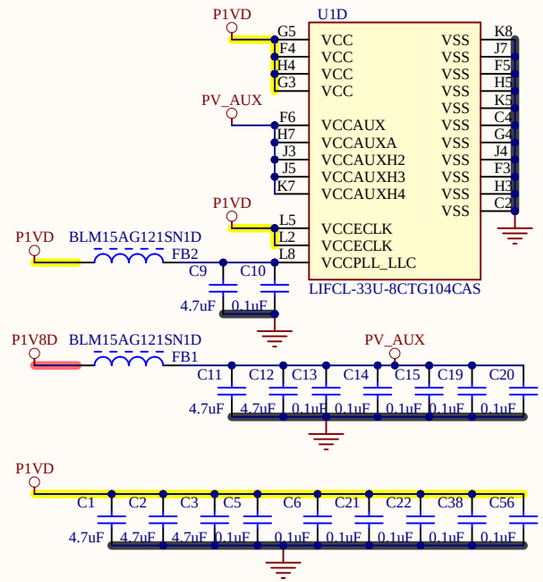
FPGA Bank 0: Flash/JTAG



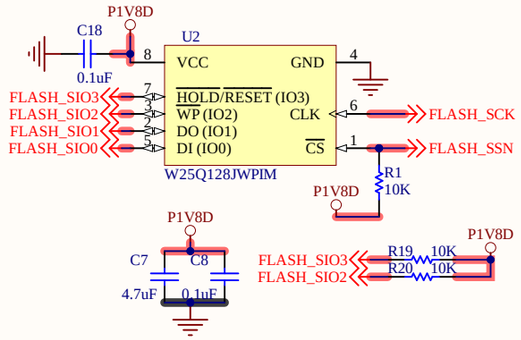
JTAG Pullups



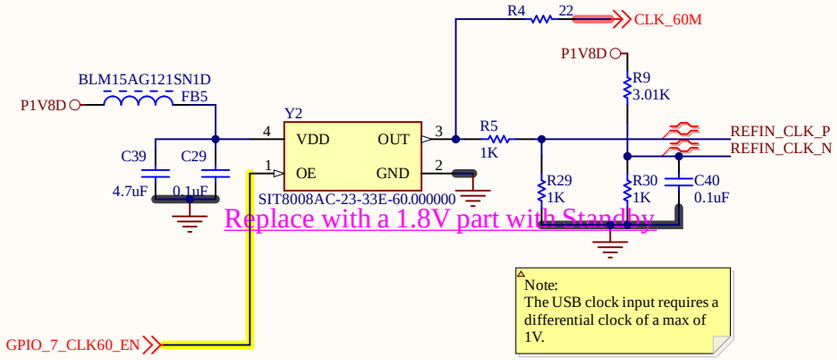
Power/Ground



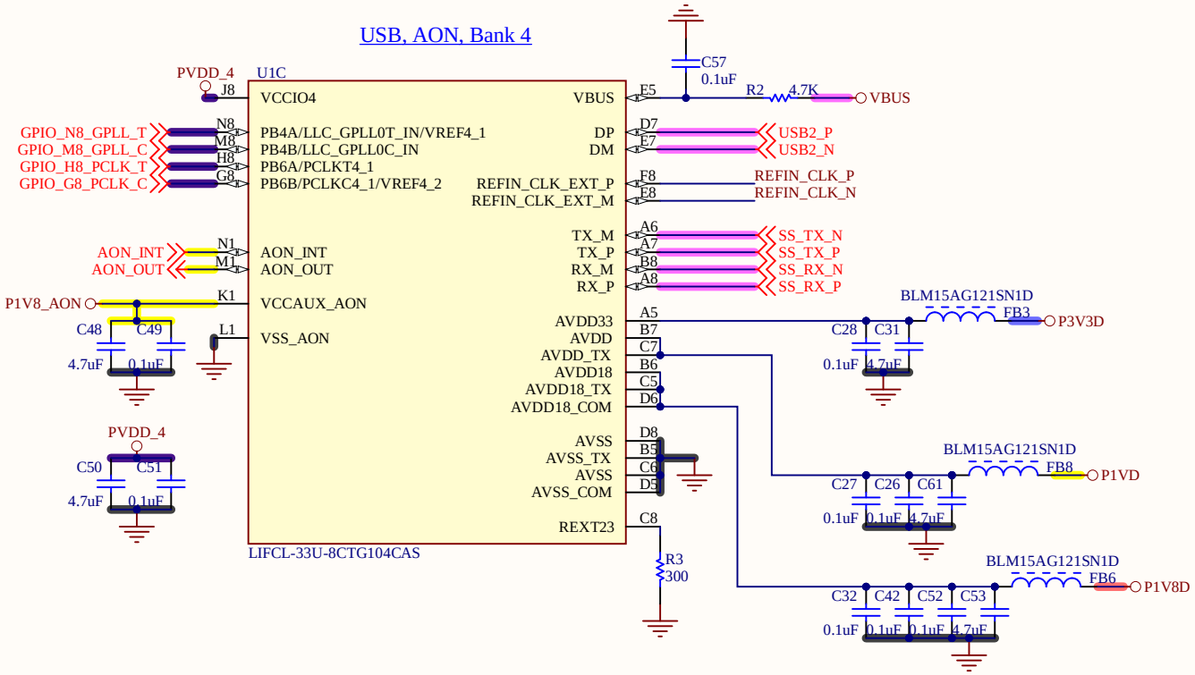
16MB qSPI Flash



Clock

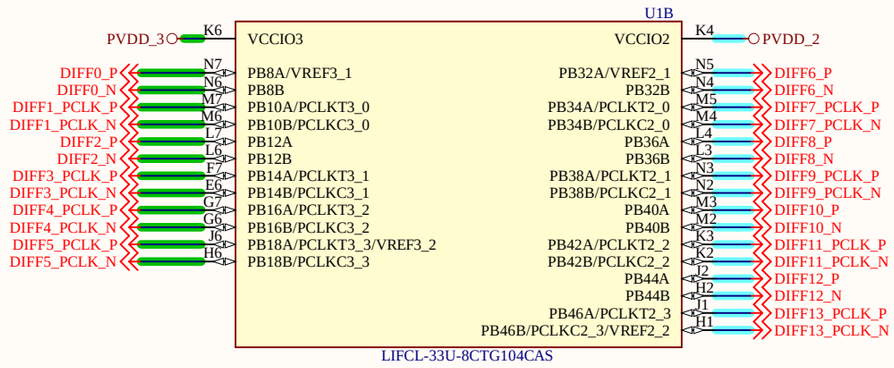


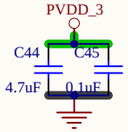
USB, AON, Bank 4

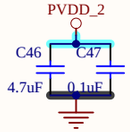


Bank 3: External Interface

Bank 2: External Interface



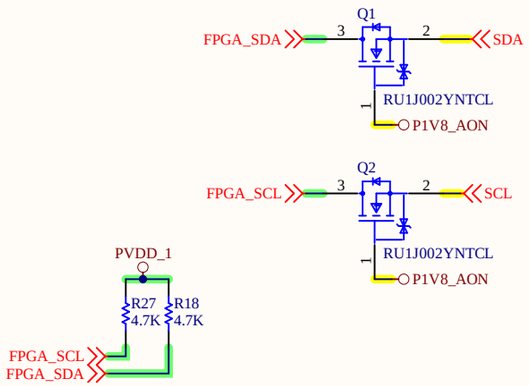




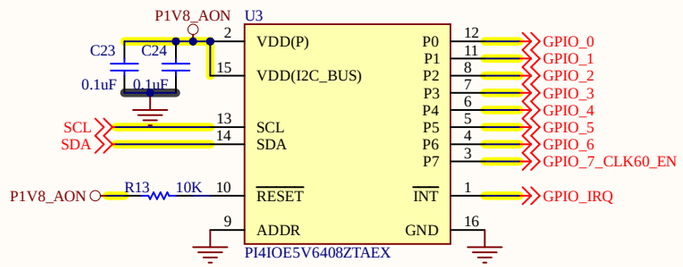
Layout: Length match all Bank 2 diff pairs with 1mm

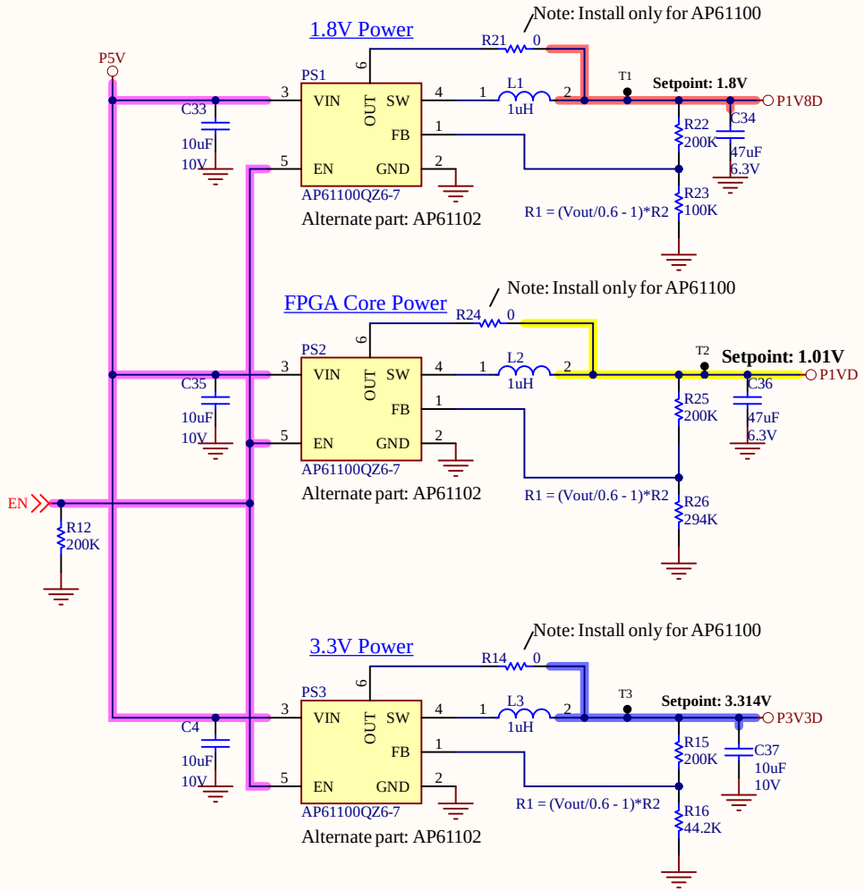
Layout: Length match SRAM_CLK to data lanes within 0.1mm

I2C Level translation



GPIO Expander





Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V