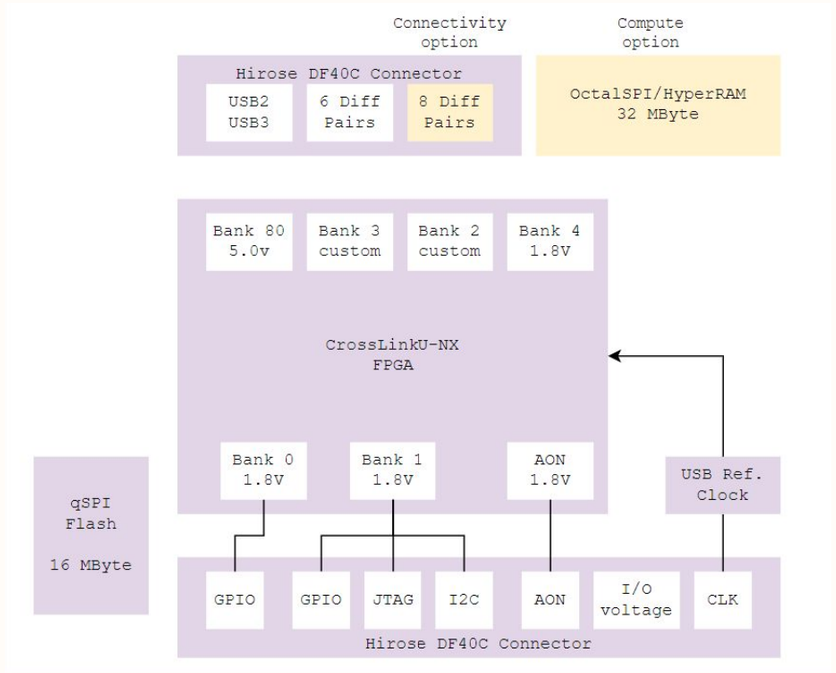
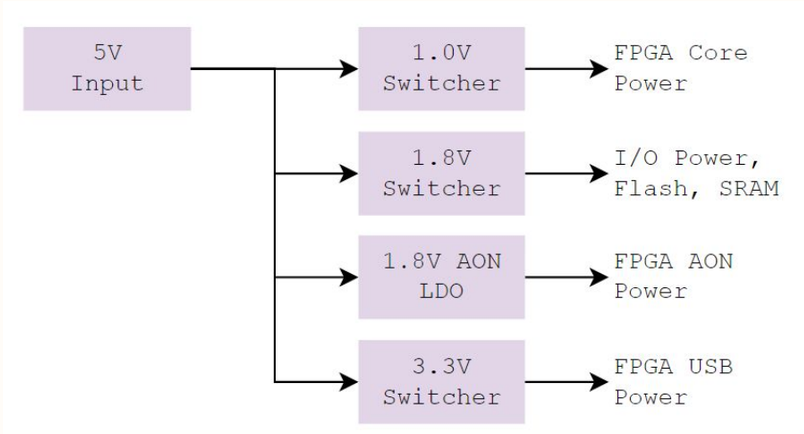
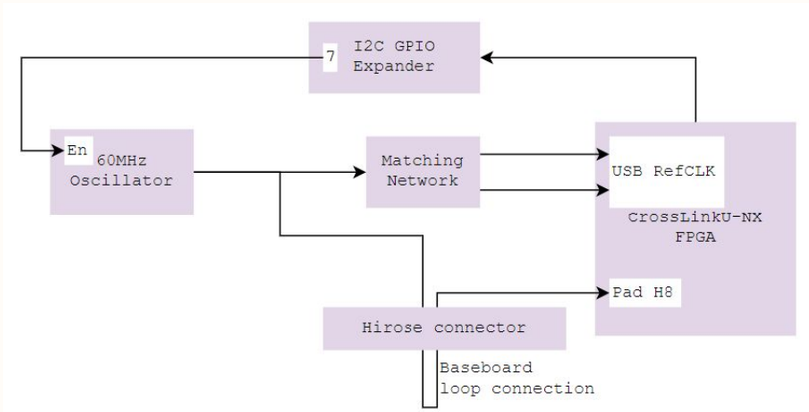
FPGA Bank Allocation



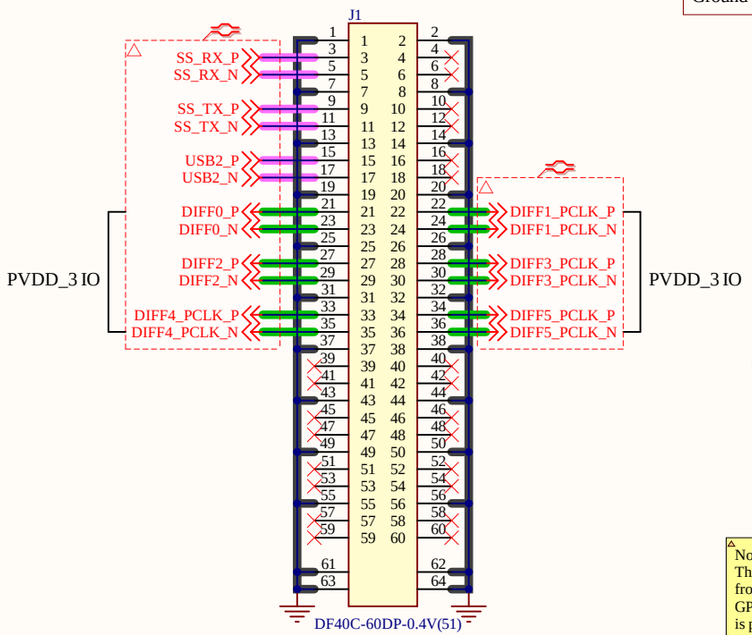
Power Distribution

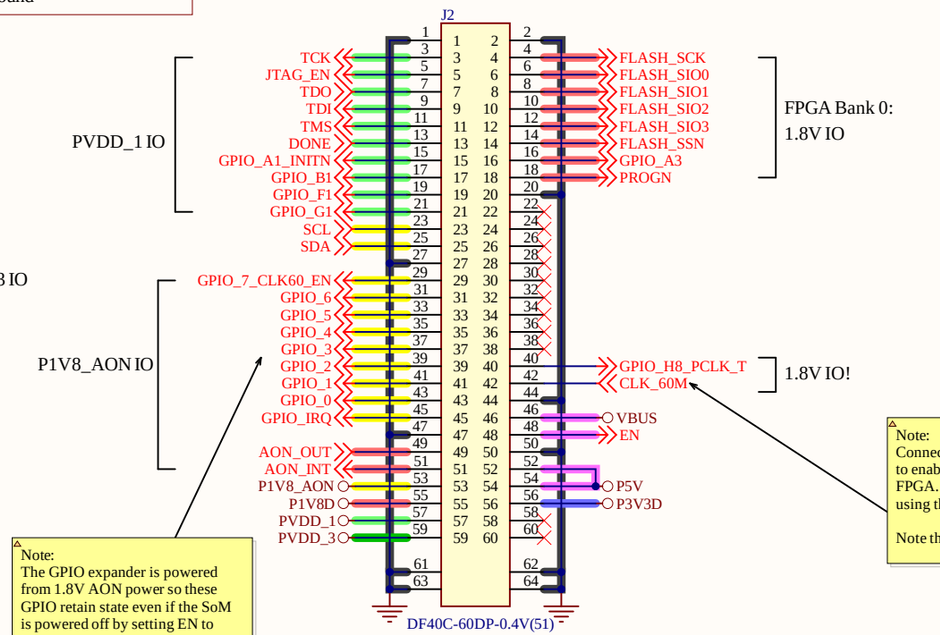


Clocking



Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Bank 3 Voltage (1.2-1.8V)
Always ON (1.8V)
Ground



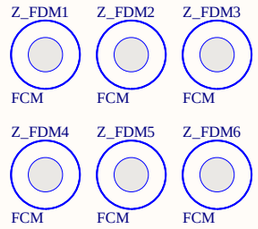


Note:
The GPIO expander is powered from 1.8V AON power so these GPIO retain state even if the SoM is powered off by setting EN to low.

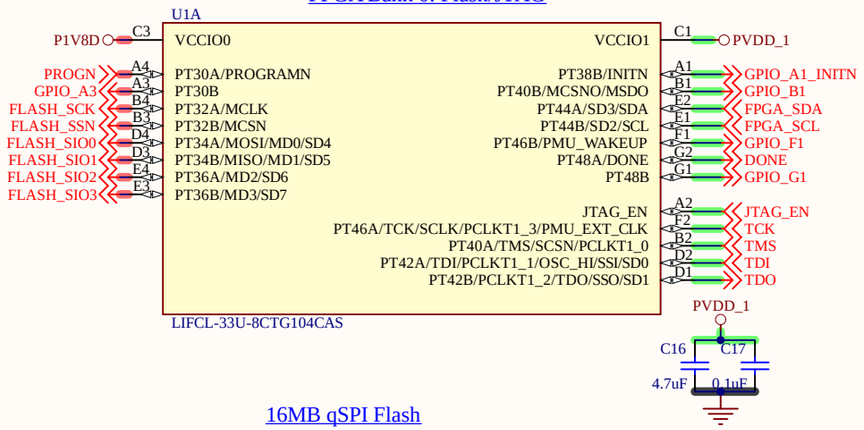
Note:
Connect CLK_60 to GPIO_H8_PCLK_T on the baseboard to enable the onboard oscillator to send a clock to the FPGA. An external clock can be supplied to the FPGA using the H8 pin.

Note that CLK_60 is 1.8V IO as is GPIO_H8_PCLK_T.

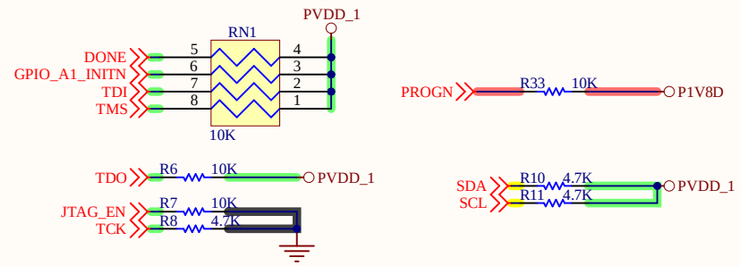
Layout note: Match diff pairs to within 1mm of each other.



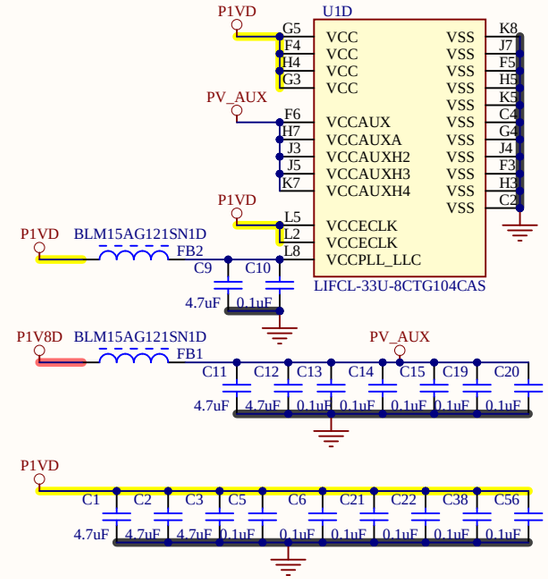
FPGA Bank 0: Flash/JTAG



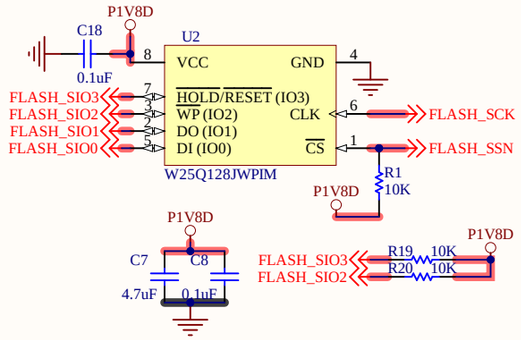
I2C and JTAG Pullups



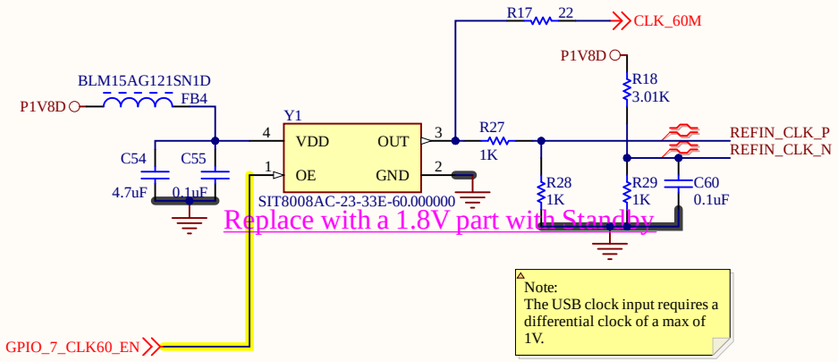
Power/Ground



16MB qSPI Flash



Clock

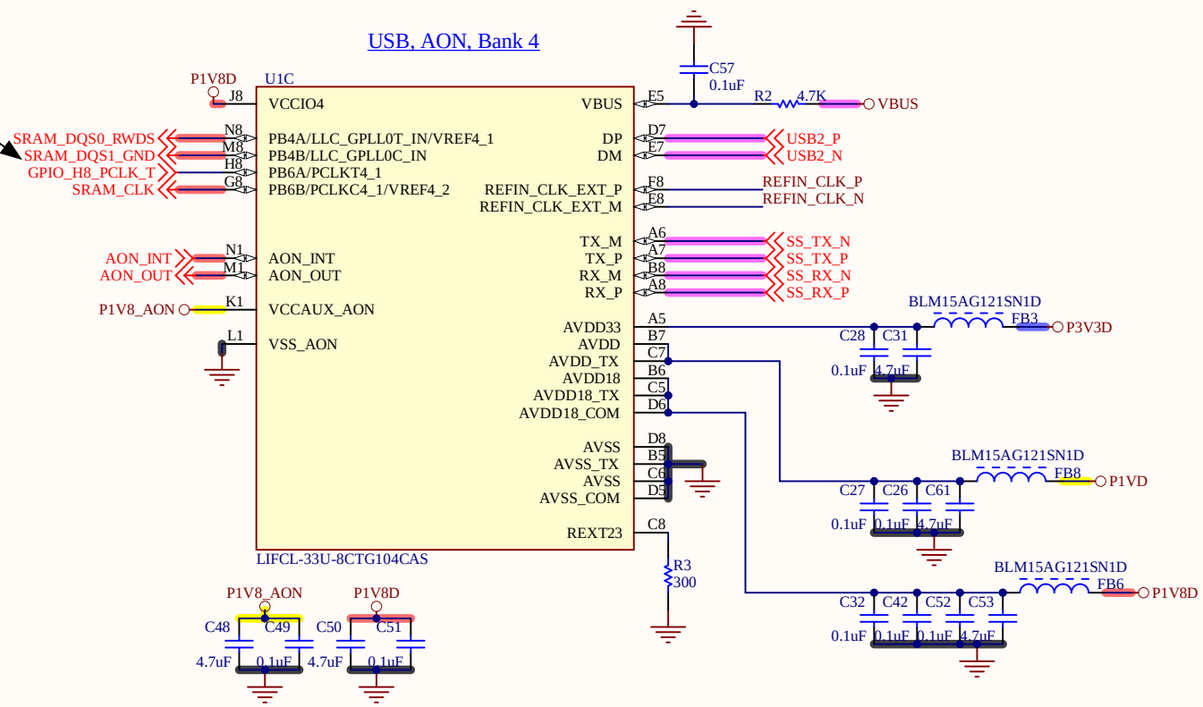


Replace with a 1.8V part with Standby

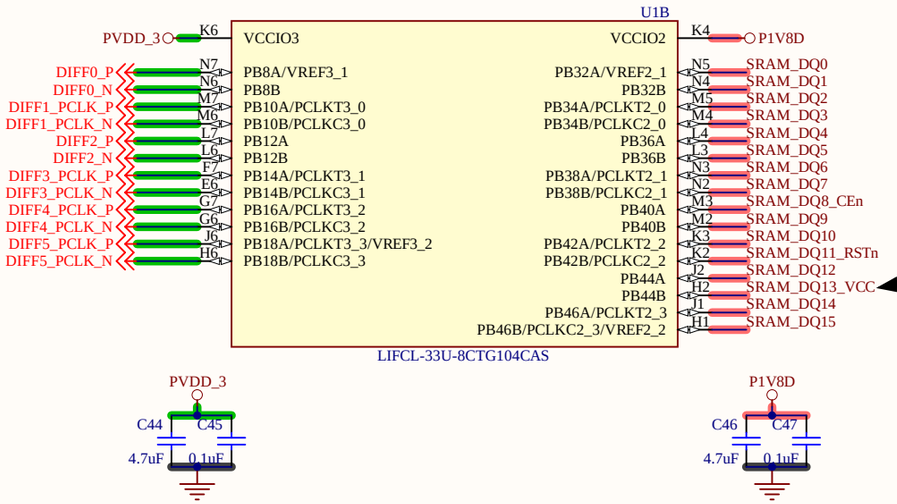
Note:
The USB clock input requires a differential clock of a max of 1V.

Note:
FPGA must set SRAM_DQS1 to ground for HyperRAM!

USB, AON, Bank 4

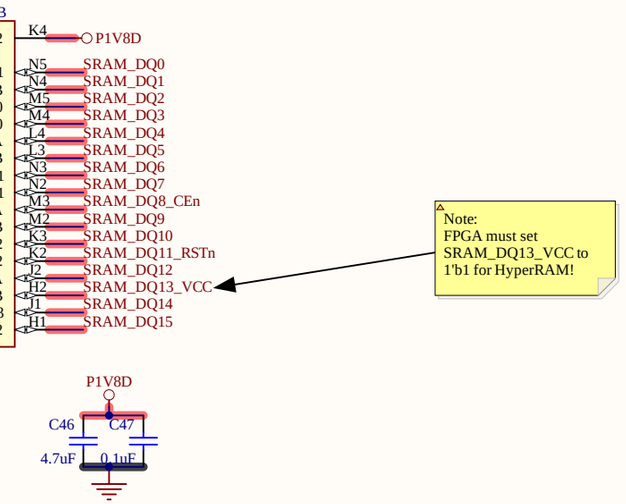


Bank 3: External Interface



Layout: Length match all Bank 2 diff pairs with 1mm

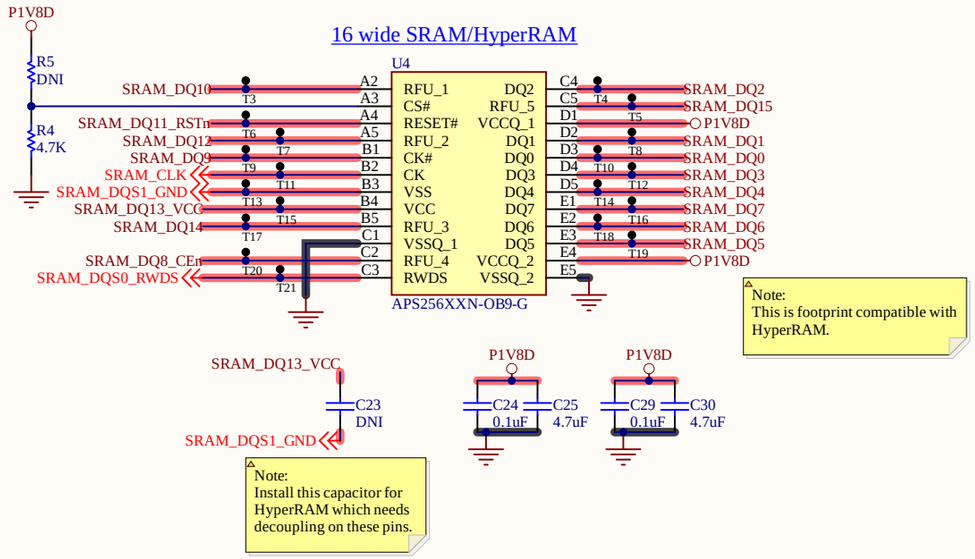
Bank 2: 32MB oSPI/HyperRAM



Note:
FPGA must set SRAM_DQ13_VCC to 1'b1 for HyperRAM!

Layout: Length match SRAM_CLK to data lanes within 0.1mm

16 wide SRAM/HyperRAM

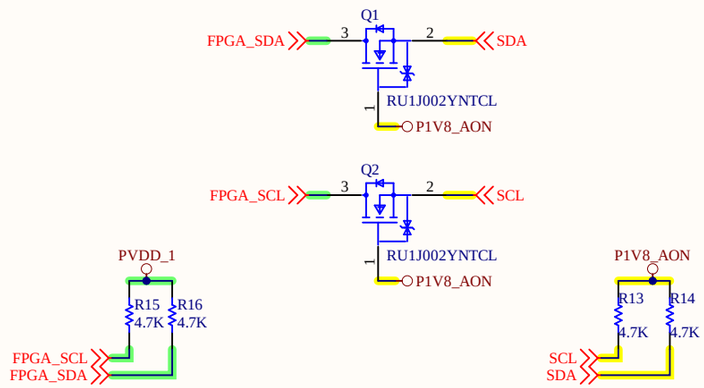


Note:
This is footprint compatible with HyperRAM.

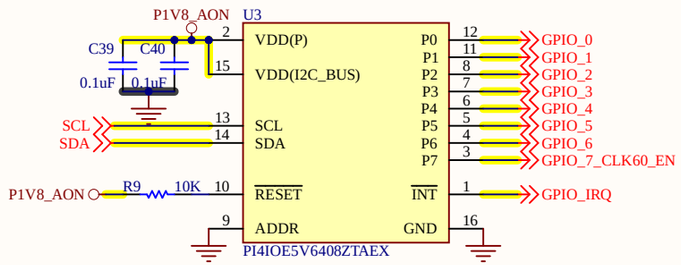
Note:
Install this capacitor for HyperRAM which needs decoupling on these pins.

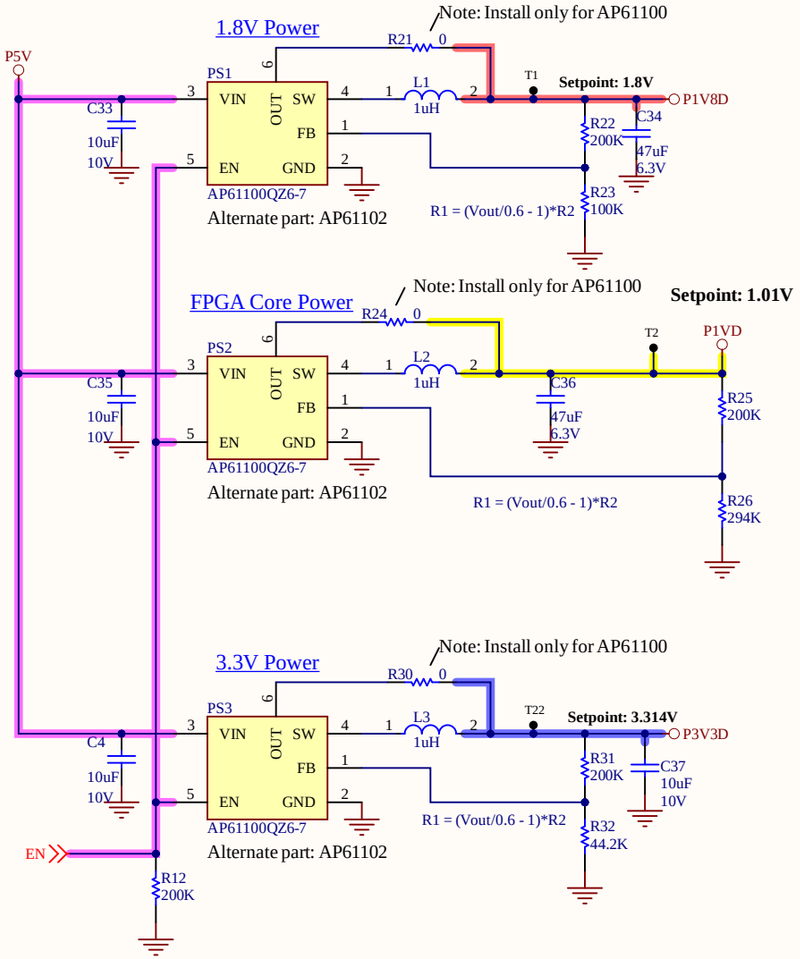
Layout: Test points on the SRAM_* nets are vias with cleared out solder mask

I2C Level translation

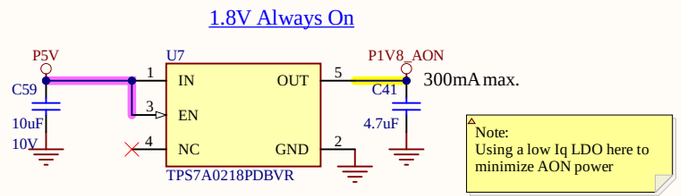


GPIO Expander





Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V



Note:
Using a low Iq LDO here to minimize AON power