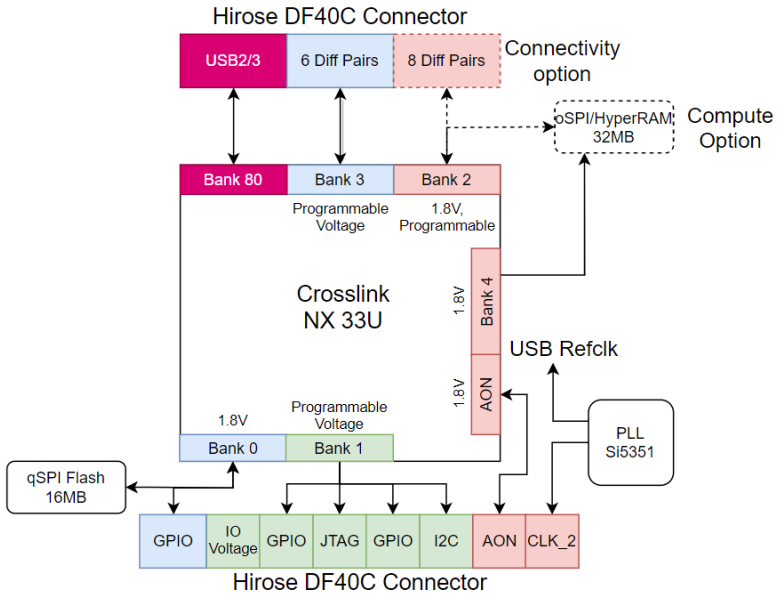
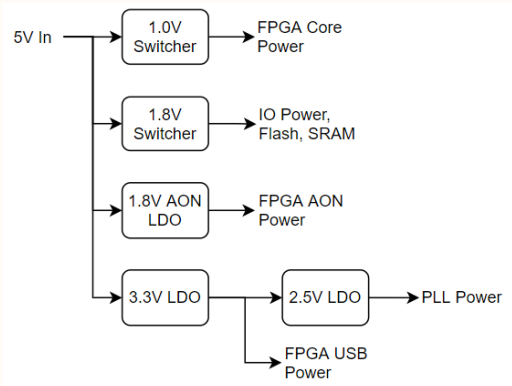
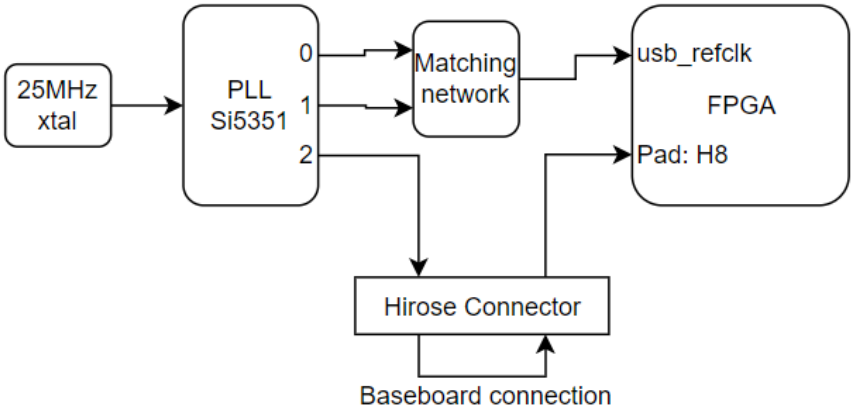
FPGA Bank Allocation



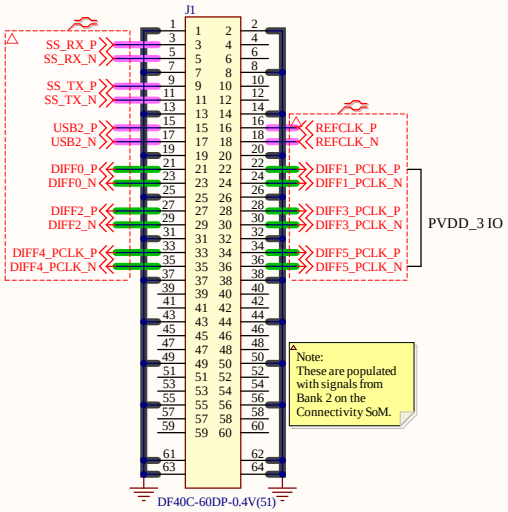
Power Distribution

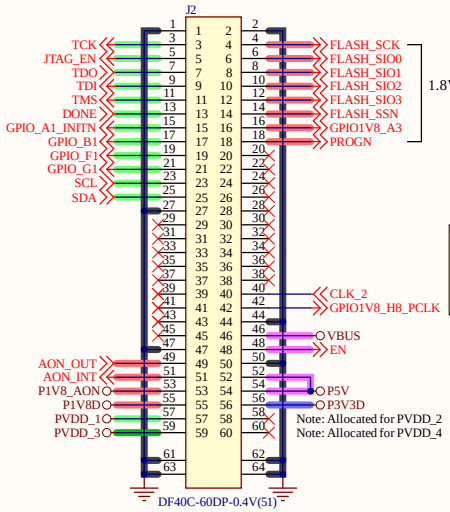


Clocking

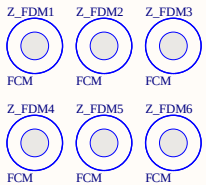


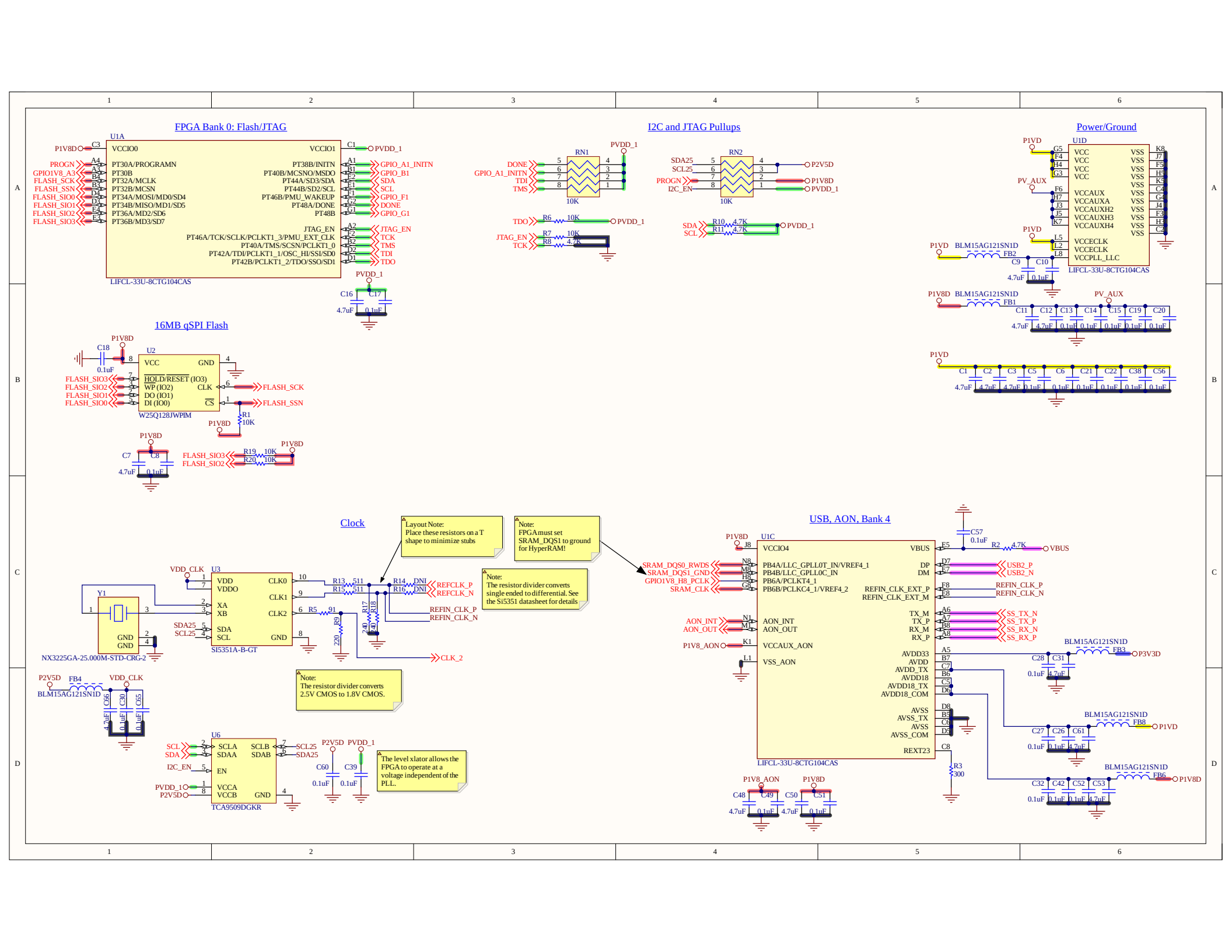
Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Bank 3 Voltage (1.2-1.8V)
Ground

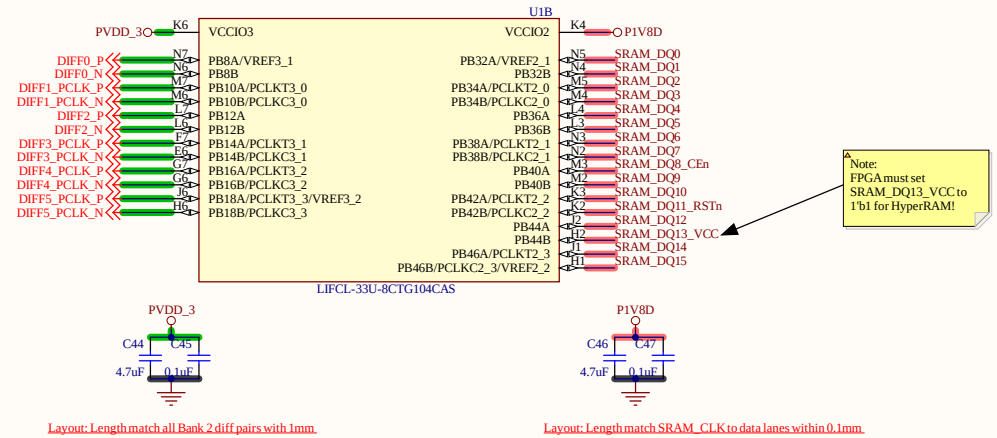


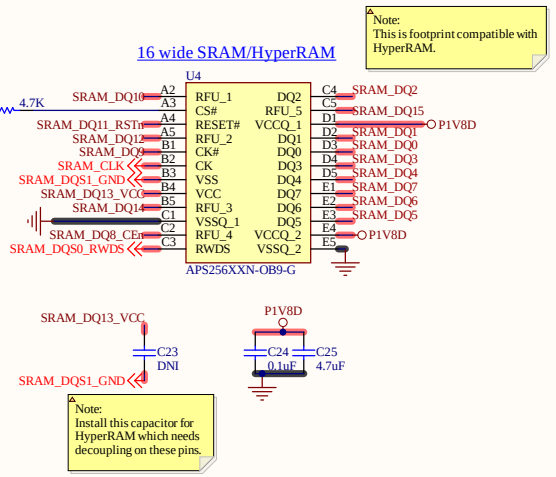


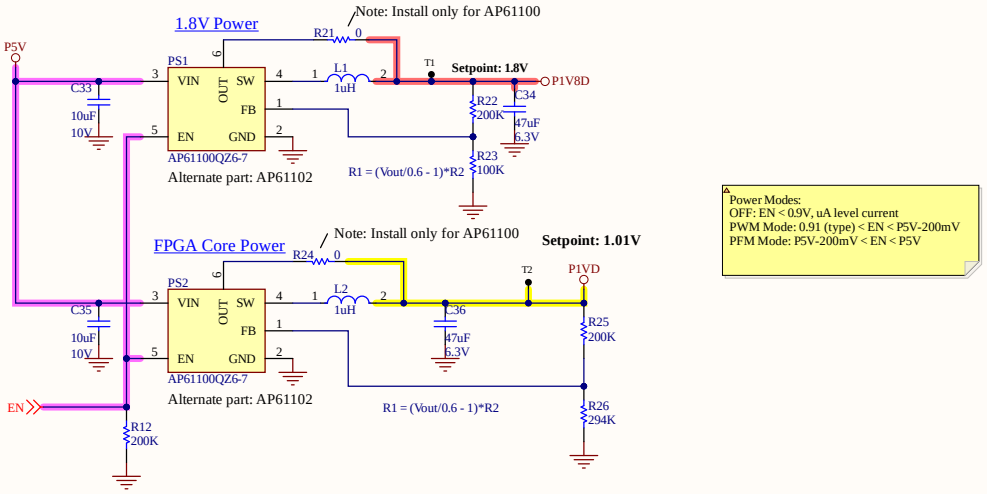
Layout note: Match diff pairs to within 1mm of each other.




FPGA Bank 0: Flash/JTAG
I2C and JTAG Pullups
Power/Ground
16MB qSPI Flash
Clock
USB, AON, Bank 4
LIFCL-33U-8CTG104CAS
W25Q128JWPIM
NX3225GA-25.000M-STD-CRG-2
SI5351A-B-GT
TCA9509DGKR
Layout Note: Place these resistors on a T shape to minimize stubs
Note: FPGA must set SRAM_DQS1 to ground for HyperRAM!
Note: The resistor divider converts single ended to differential. See the Si5351 datasheet for details
Note: The resistor divider converts 2.5V CMOS to 1.8V CMOS.
The level xlator allows the FPGA to operate at a voltage independent of the PLL.


Bank 3: External Interface
Bank 2: 32MB oSPI/HyperRAM
U1B
PVDD_3
K6
VCCIO3
VCCIO2
K4
P1V8D
DIFF0_P
DIFF0_N
DIFF1_PCLK_P
DIFF1_PCLK_N
DIFF2_P
DIFF2_N
DIFF3_PCLK_P
DIFF3_PCLK_N
DIFF4_PCLK_P
DIFF4_PCLK_N
DIFF5_PCLK_P
DIFF5_PCLK_N
PB8A/VREF3_1
PB8B
PB10A/PCLKT3_0
PB10B/PCLKC3_0
PB12A
PB12B
PB14A/PCLKT3_1
PB14B/PCLKC3_1
PB16A/PCLKT3_2
PB16B/PCLKC3_2
PB18A/PCLKT3_3/VREF3_2
PB18B/PCLKC3_3
PB32A/VREF2_1
PB32B
PB34A/PCLKT2_0
PB34B/PCLKC2_0
PB36A
PB36B
PB38A/PCLKT2_1
PB38B/PCLKC2_1
PB40A
PB40B
PB42A/PCLKT2_2
PB42B/PCLKC2_2
PB44A
PB44B
PB46A/PCLKT2_3
PB46B/PCLKC2_3/VREF2_2
SRAM_DQ0
SRAM_DQ1
SRAM_DQ2
SRAM_DQ3
SRAM_DQ4
SRAM_DQ5
SRAM_DQ6
SRAM_DQ7
SRAM_DQ8_CEn
SRAM_DQ9
SRAM_DQ10
SRAM_DQ11_RSTn
SRAM_DQ12
SRAM_DQ13_VCC
SRAM_DQ14
SRAM_DQ15
Note:
FPGA must set
SRAM_DQ13_VCC to
1'b1 for HyperRAM!
LIFCL-33U-8CTG104CAS
PVDD_3
C44
C45
4.7uF
0.1uF
P1V8D
C46
C47
4.7uF
0.1uF
Layout: Length match all Bank 2 diff pairs with 1mm
Layout: Length match SRAM_CLK to data lanes within 0.1mm


16 wide SRAM/HyperRAM
Note:
This is footprint compatible with
HyperRAM.
U4
R4
4.7K
SRAM_DQ10
SRAM_DQ11_RSTn
SRAM_DQ12
SRAM_DQ9
SRAM_CLK
SRAM_DQS1_GND
SRAM_DQ13_VCC
SRAM_DQ14
SRAM_DQ8_CEn
SRAM_DQS0_RWDS
RFU_1
CS#
RESET#
RFU_2
CK#
CK
VSS
VCC
RFU_3
VSSQ_1
RFU_4
RWDS
DQ2
RFU_5
VCCQ_1
DQ1
DQ0
DQ3
DQ4
DQ7
DQ6
DQ5
VCCQ_2
VSSQ_2
SRAM_DQ2
SRAM_DQ15
P1V8D
SRAM_DQ1
SRAM_DQ0
SRAM_DQ3
SRAM_DQ4
SRAM_DQ7
SRAM_DQ6
SRAM_DQ5
P1V8D
APS256XXN-OB9-G
SRAM_DQ13_VCC
C23
DNI
SRAM_DQS1_GND
P1V8D
C24
0.1uF
C25
4.7uF
Note:
Install this capacitor for
HyperRAM which needs
decoupling on these pins.



Power Modes:
OFF: EN < 0.9V, uA level current
PWM Mode: 0.91 (type) < EN < P5V-200mV
PFM Mode: P5V-200mV < EN < P5V