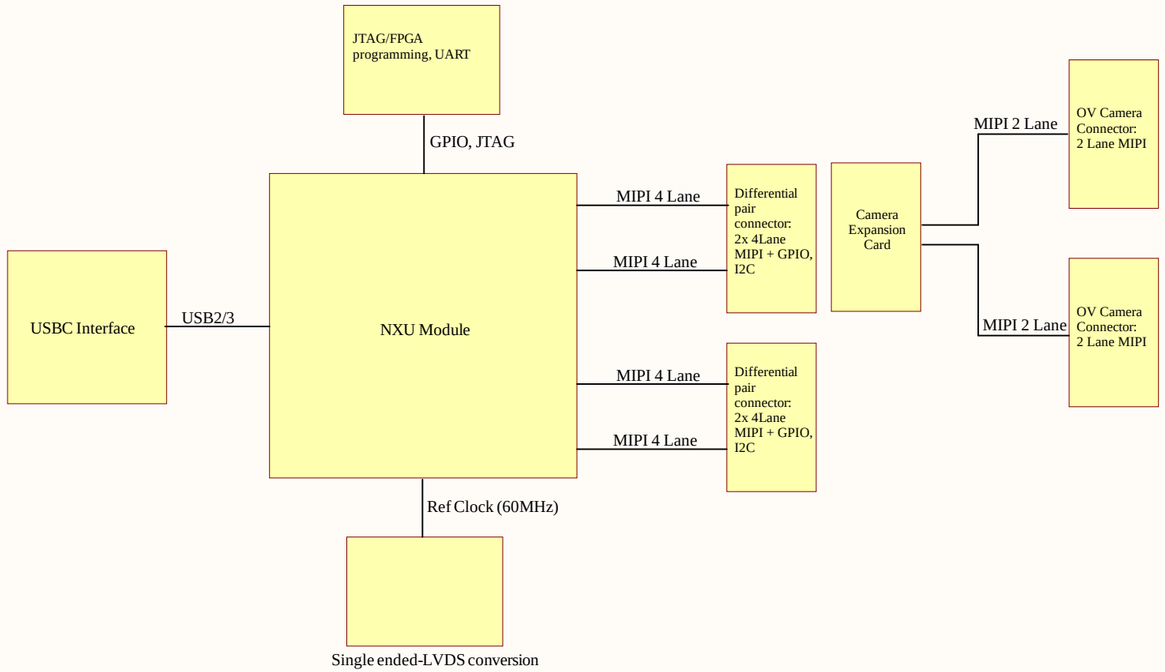
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT

Altium™

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE

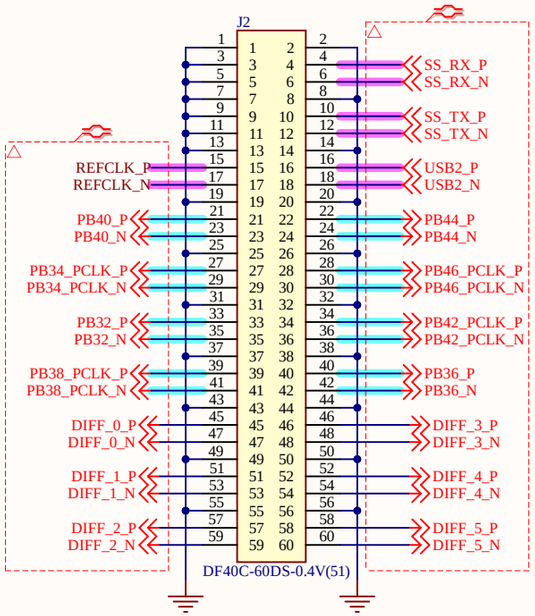
*

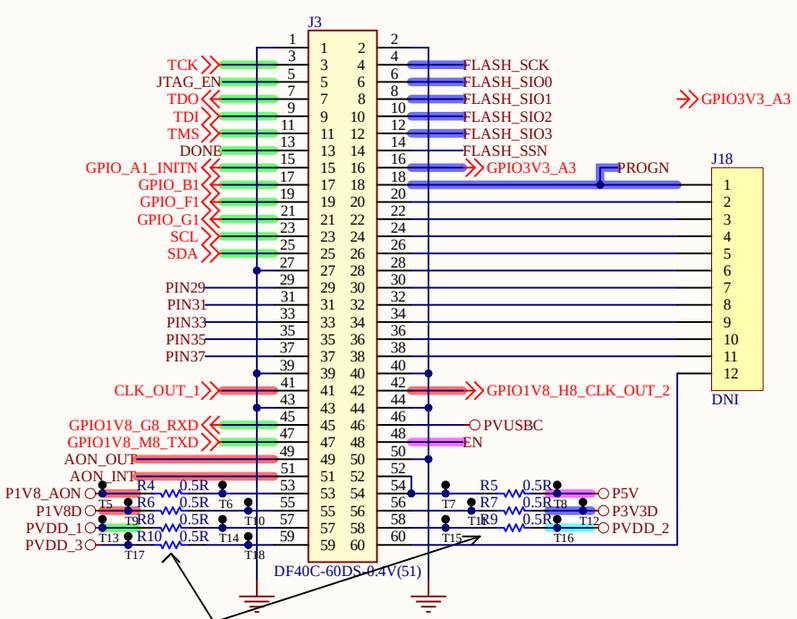
SIZE	CAGE CODE	DWG NO.	REV
B			

SCALE: | FILE NAME Overview.SchDoc | SHEET 1 OF 4

Color Legend:
3.3V IO
USB
1.8V
Bank 1 Voltage (1.2-3.3V)
Bank 2 Voltage (1.2-1.8V)
Ground

SoM Connectors

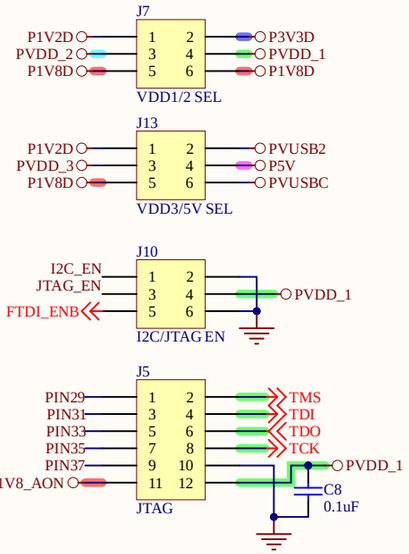


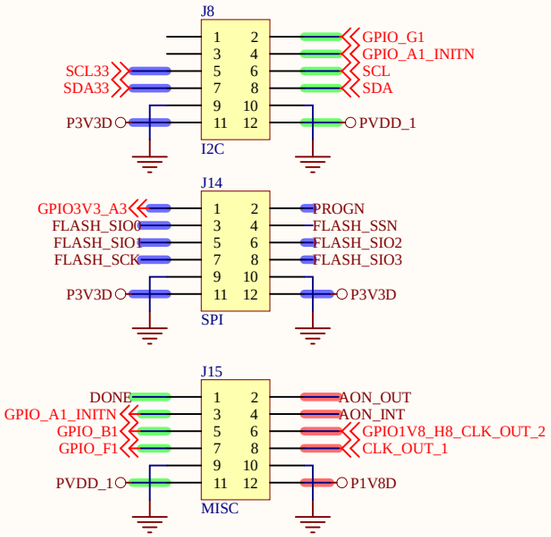


Layout note: Place these resistors in an accessible location

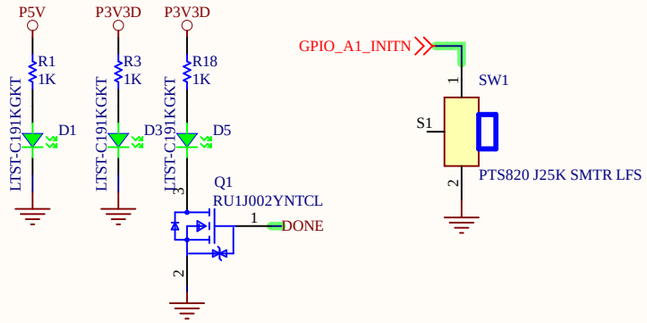
Reserved for Future use:
These signals will end up allocated to Bank 3 and the whole bank will be brought out to these pins when there is no SSRAM installed.

Debug Ports

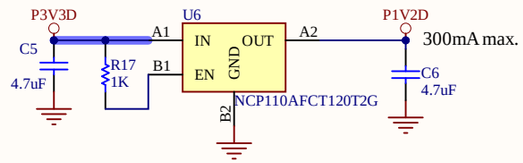




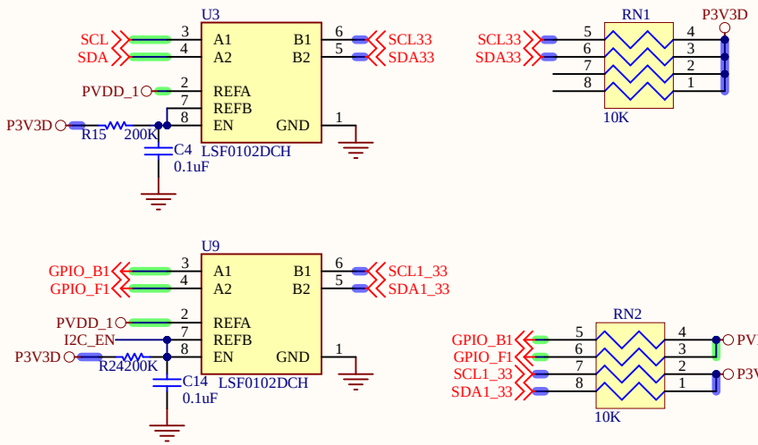
LED's/Switch



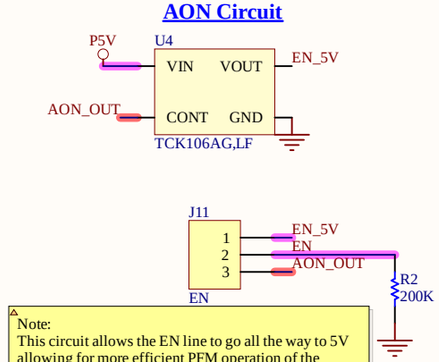
1.2V LDO



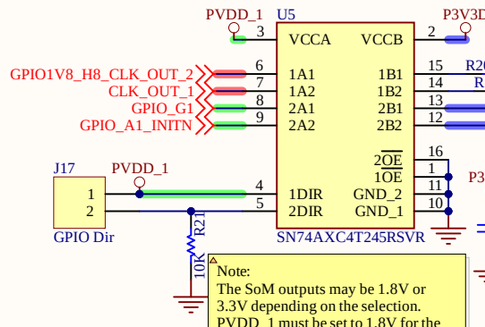
I2C Level translator



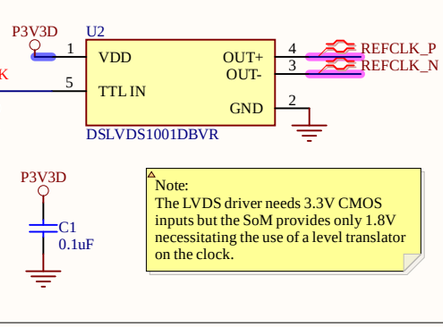
AON Circuit



1.8V-3.3V Level translator



USB Reference Clock



PCB LOGO
WEEE

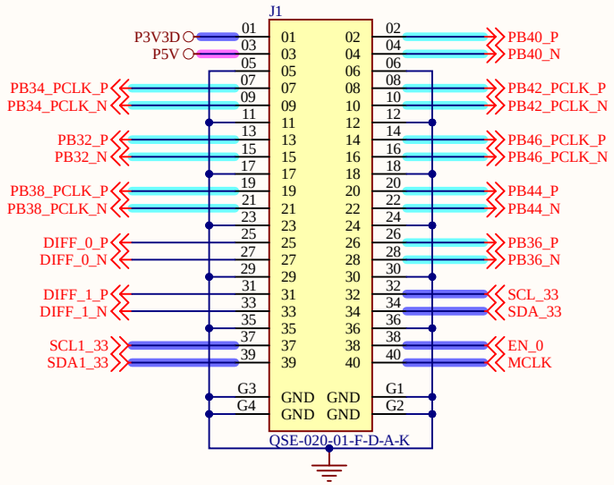
PCB LOGO
ESD Susceptible

TP1

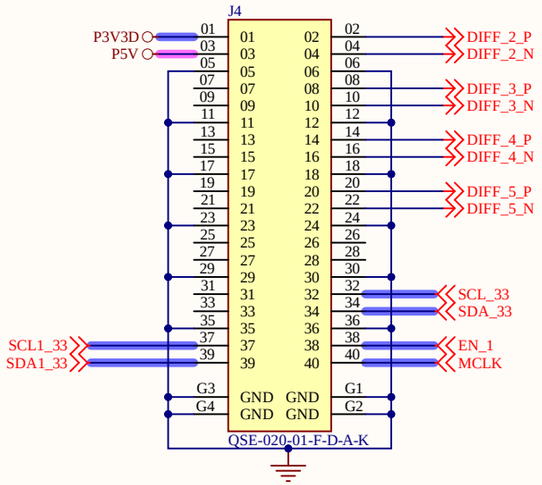
1 FID
1 FID
1 FID

Title	tinyNX33U Module BaseBoard	
Size: B	Number:	Revision:
Date: 7/17/2023	Sheet of	
File: E:\@@@@@Darial\..\Base_Module.SchDoc	Drawn By:	

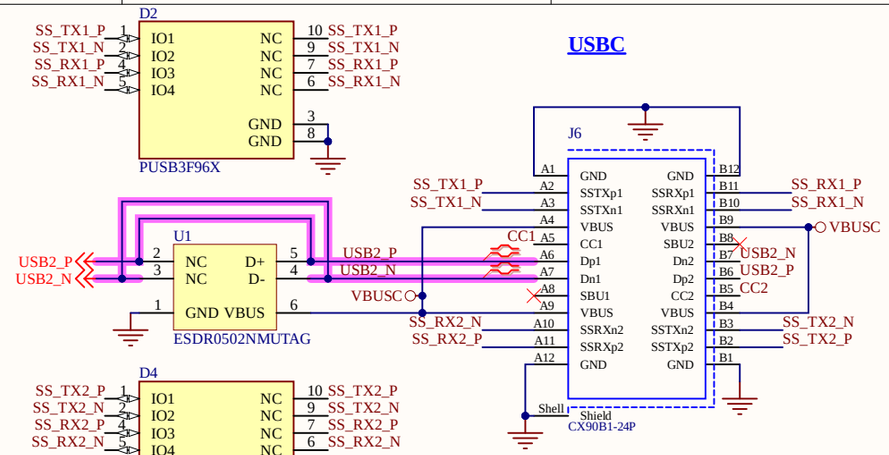
Expansion Connector A

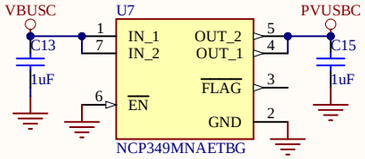


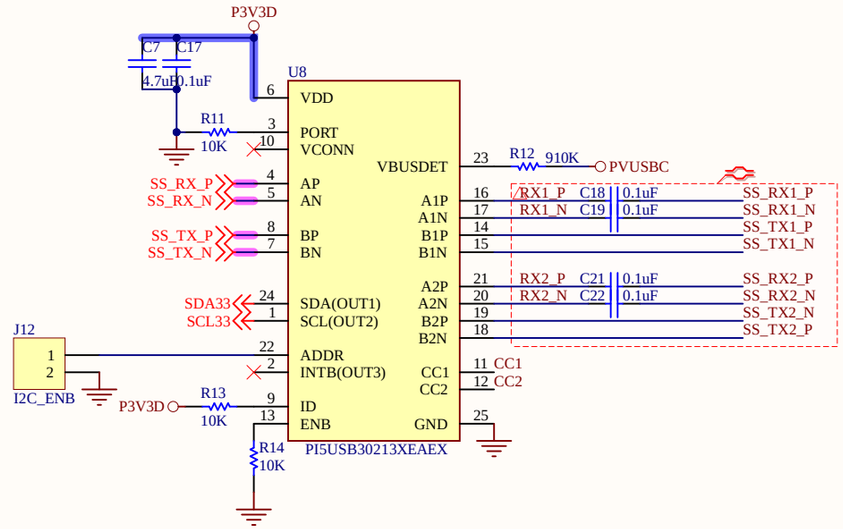
Expansion Connector B



USBC

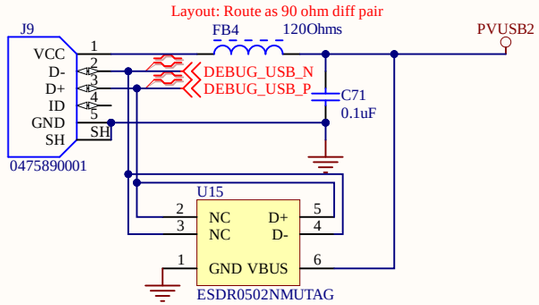




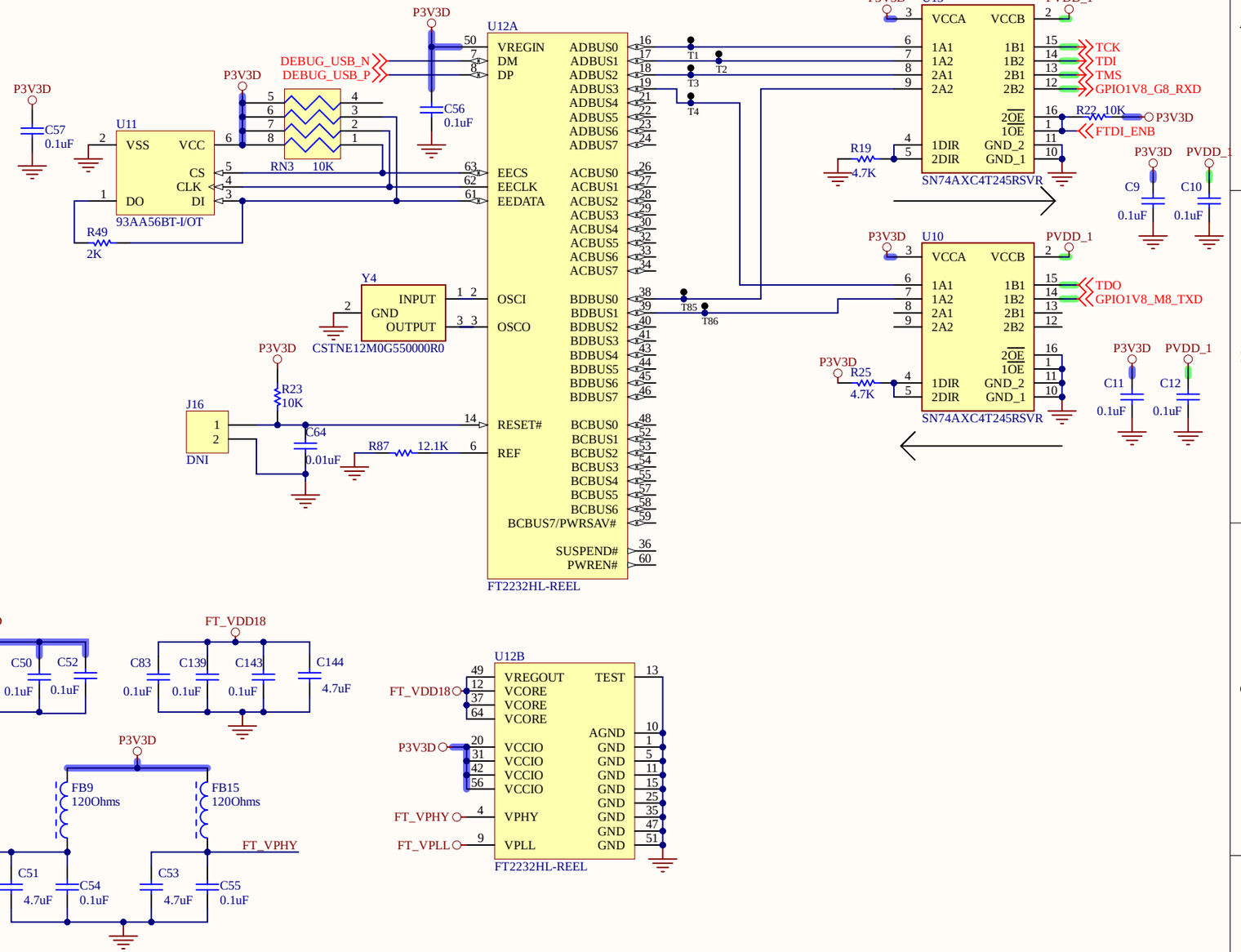


Title: tinyNX33U Module BaseBoard		
Size: B	Number:	Revision:
Date: 7/17/2023	Sheet of	
File: E:\@@@@@Darial\..\Base_USB_Camera_Dual.Ddb	Drawn By:	

Debug/Programming USB



FPGA Programmer



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